AMENDMENTS TO THE SPECIFICATION:

Page 1, between the Title and first paragraph, add the following paragraph and headings:

This application is the US national phase of International Application No. PCT/GB99/04275, filed 16 December 1999, the entire content of which is hereby incorporated by reference.

BACKGROUND OF THE INVENTION

1. Field of the Invention

Page 1, amend the paragraph beginning at line 4 as follows:

2. Discussion of Prior Art

The spatial light modulator to be described in relation to a preferred embodiment in this specification is a in the form of a smectic liquid crystal layer disposed between an active semiconductor backplane and a common front electrode. It was developed in response to a requirement for a fast and, if possible, inexpensive, spatial light modulator comprising a relatively large number of pixels with potential application not only as a display device, but also for other forms of optical processing such as correlation and holographic switching. Other aspects of this device are dealt with in our copending International Patent Applications of even filing and priority dates (PCT/GB99/04285, ~~ref: P20957WO~~U.S. Serial No. 09/868,219, priority GB9827952.4; PCT/GB99/04286 and PCT/GB99/04276, ~~refs: P20958WO and P20958WO1~~U.S. Serial No. 09/868,230 and

U.S. Serial No. 09/868,220, both priority GB9827965.6; PCT/GB99/04282, ~~ref: P20959WO~~U.S. Serial Nos. 09/446,325 and 10/084,652, priority GB9827900.3; PCT/GB99/04279, ~~ref: P20960WO~~U.S. Serial No. 10/085,140, priority GB9827901.1; PCT/GB99/04274, ~~ref: P20961WO~~U.S. Serial Nos 09/868,218 and 10/094,958, priority GB9827964.9; and PCT/GB99/04260 and PCT/GB99/04277, ~~refs: P20963WO and P20963WO1~~U.S. Serial No. 09/868,242, both priority GB 9827944.1).

Page 4, amend the paragraph beginning at line 26 as follows:

In contrast to the type of RAM associated with computing, the pixel circuits, and more significantly the pixel transistors, are often at least partially exposed to light. This can lead to problems, especially with DRAM type backplanes where the pixels are part of the DRAM circuit, including photo-induced conductivity and charge leakage. This aspect is dealt with in greater detail in our copending application PCT/GB99/04279, ~~ref: P20960WO~~U.S. Serial No. 10/085,140.

Page 6, amend the paragraph beginning at line 8 as follows:

However, as the liquid crystal thickness approaches the thicknesses associated with the underlying structure of the backplane, and any possible deformation of the liquid crystal cell structure by flexing or other movement of the substrates, problems arise, for example as to the uniformity of response across the pixel area, and the capability for short circuiting across the cell thickness. These factors are dealt with in more detail in our

copending applications PCT/GB99/04285, ~~ref: P20957WO~~U.S. Serial No. 09/868,219; and PCT/GB99/04282, ~~ref: P20959WO~~U.S. Serial Nos. 09/446,325 and 10/084,652.

Page 7, amend the paragraph beginning at line 5 as follows:

One solution is to provide an additional "slug" capacitance which is rapidly charged during the addressing pulse and so can provide a reservoir of charge while the capacitive element switches over a longer time period. This aspect is dealt with in more detail in our copending application PCT/GB99/04279, ~~ref: P20960WO~~U.S. Serial No. 10/085,140, which relates to the provision of a semiconductor active backplane including an array of addressable active elements on a semiconductor substrate for energising respective first electrodes, wherein at least part of the region beneath a said electrode is adapted to act as a capacitor. In particular said part may be formed as a depletion region whereby in use it acts as a reverse biassed diode, or individual capacitor plates may be formed beneath the electrode, one coupled to the substrate and the other coupled to the electrode.

Page 12, amend the paragraph beginning at line 11 as follows:

Our copending application PCT/GB99/04274, ~~ref: P20961WO~~U.S. Serial Nos. 09/868,218 and 10/094,958 relates to the provision of an array of electrically addressable elements, said array comprising a plurality of mutually exclusive sets of said elements, means arranged to address said sets one at a time, and means for addressing more than one (and preferably all) of said plurality of sets (the "selected sets") simultaneously.

While the most common form of array is arranged as addressable rows (the sets) and columns, other arrangements are possible, for example based on polar co-ordinates (distance and angle). However. modern computing methods and standards converters have tended to make other formats redundant in the majority of cases.

Page 12, above the paragraph beginning at line 24, insert the following heading:

SUMMARY OF THE INVENTION

Page 15, above the paragraph beginning at line 13, insert the following heading:

BRIEF DESCRIPTION OF THE DRAWINGS

Page 16, amend the paragraph beginning at line 23 as follows:

~~Figure 13 shows~~Figures 13a and 13b show waveforms used to illustrate a one-pass image writing scheme; and

Page 16, amend the paragraph beginning at line 26 as follows:

Figure ~~15~~17 shows waveforms for illustrating a modification of the scheme of Figures ~~14~~14-16.

Page 17, above the paragraph beginning at line 1, insert the following heading:

DETAILED DISCUSSION OF EMBODIMENTS

Page 18, amend the paragraph beginning at line 8 as follows:

Odd and even row conductors are connected 21 to respective scanners 44, 45 spaced either side of the array. Each scanner comprises a level shifter 44b, 45b

interposed between a shift register 44a, 45a and the array. In use, a token signal is passed along the registers to enable (render the associated transistors conductive) individual rows in turn, and by suitable control of the registers different types of scan, e.g. interlaced or non-interlaced, can be performed as desired.

Page 18, amend the paragraph beginning at line 14 as follows:

Odd and even column conductors are connected 22 to respective drivers 42, 43 spaced from the top and bottom of the array. Each driver comprises a 32 to 160 demultiplexer 42a, 43a feeding latches 42b, 43b, and a level shifter 42c, 43c between the latches and the column conductors. In use, under the control of a 5-phase clock, data from the memory 24 for successive sets of 32 odd or even column conductors is passed from sets of edge bonding pads 46, 47 to the demultiplexers 42a, 43a, and latched at 42b, 43b before being level shifted at 42c, 43c for supply as a driving voltage to the column conductors. Synchronisation between the row scanning and column driving ensures that the appropriate data driving voltage is applied via the enabled transistors of a row to the liquid crystal pixels, and for this purpose various control circuits 48 are provided.

Page 21, amend the paragraph beginning at line 19 as follows:

In Figures 5 and 6, step (a) is implemented insofar as the transistor 52, and particularly its gate region, is located substantially beneath metallic conductors 60, 61 and in that the diode provided by region 66, which is especially photosensitive, is largely hidden by the mirror layer 65. Further details regarding the slug capacitance and the

avoidance of photoconductive effects will be found in our copending application PCT/GB99/04279, ~~ref: P20960WO~~U.S. Serial No. 10/085,140.

Page 28, amend the paragraph beginning at line 4 as follows:

(a) Binary/Grey Scale Thus, for example, there is a choice between binary and grey scale modulation. Grey scale modulation itself may be achieved either in an analogue manner by suitable control of the amplitude voltage applied across each pixel (cf the electroclinic effect mentioned earlier), but advantageously for display purposes the array is subject to variable temporal modulation to provide an apparent grey scale. Even more advantageously, the array is so driven on a digital basis. This aspect is covered in more detail below and also in our copending application PCT/GB99/04260, ~~ref: P20963WO~~U.S. Serial No. 09/868,242.

Page 35, amend the paragraph beginning at line 30 and continuing to page 36, line 3 as follows:

Although the above and other imaging schemes herein have been illustrated as employing global blanks, it should be noted that any or all of the blanks could be replaced by a further frame scan in which all columns are held at the blanking voltage. This provision of circuitry enabling a global addressing step forms the subject of our copending application PCT/GB99/04274, ~~ref: P20961WO~~U.S. Serial Nos. 09/868,218 and 10/094,958.

Page 38, amend the paragraph beginning at line 6 as follows:

There are other schemes, the subject of our copending application PCT/GB99/04260, ~~ref: P20963WO~~U.S. Serial No. 09/868,242 in which dc balance is approached or achieved in ways other than be employing dc balanced binary images per se.